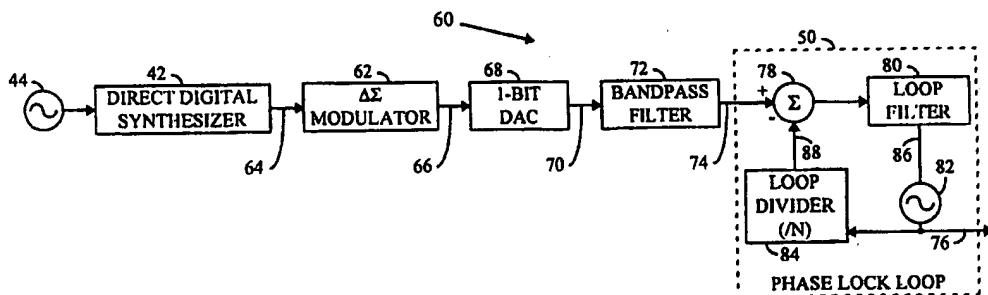




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : H03L 7/18, G06F 1/02		A1	(11) International Publication Number: WO 00/01072 (43) International Publication Date: 6 January 2000 (06.01.00)
(21) International Application Number: PCT/US99/14655			(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).
(22) International Filing Date: 29 June 1999 (29.06.99)			
(30) Priority Data: 09/107,868 30 June 1998 (30.06.98) US			
(71) Applicant: QUALCOMM INCORPORATED [US/US]; 6455 Lusk Boulevard, San Diego, CA 92121 (US).			
(72) Inventors: BUTTERFIELD, Daniel, Keyes; 12803 Calle De La Siena, San Diego, CA 92130 (US). GILMORE, Robert, P.; 12411 Ragweed Street, San Diego, CA 92129 (US).			
(74) Agents: MILLER, Russell, B. et al.; Qualcomm Incorporated, 6455 Lusk Boulevard, San Diego, CA 92121 (US).			
			Published <i>With international search report.</i>

(54) Title: SYSTEM FOR GENERATING AN ACCURATE LOW-NOISE PERIODIC SIGNAL



(57) Abstract

In the illustrative embodiment, the inventive system includes a low-bit digital-to-analog converter (68) for converting a first signal at a reference frequency to a digital signal. A delta-sigma converter is included for suppressing noise in the digital signal within the predetermined range of the reference frequency and providing a noise-shaped signal in response thereto. A bandpass filter (72) filters out the out-of-band noise and provides an accurate periodic signal which lacks glitch noise. In a particular embodiment, the inventive system further includes a direct digital synthesizer (42) for providing the first signal at the first frequency and the accurate reference periodic signal is supplied as reference signal to a phase-locked loop (50).

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SYSTEM FOR GENERATING AN ACCURATE LOW-NOISE PERIODIC SIGNAL

5

BACKGROUND OF THE INVENTION

I. Field of the Invention

10 This invention relates to communication systems. Specifically, the present invention relates to systems and techniques for generating accurate low noise periodic signals for use in communication systems.

15 II. Description of the Related Art

Periodic electronic signals are used in variety of demanding applications including reference oscillators used to modulate and demodulate signals in analog circuits and clocks for digital circuits. Such applications often require very accurate low-noise signals that consume 20 minimal power while maintaining accuracy over a range of frequencies.

The accuracy of such signals are particularly important in digital communications systems such as code division multiple access (CDMA) communications systems. In CDMA systems, signals within a certain range of frequencies must often be translated to a different range or band of 25 frequencies. The accuracy of the clock signal affects the accuracy of the frequency translation. For example in a CDMA cellular telephone network, a local oscillator (LO) in a mobile receiver provides a periodic signal that facilitates the translation of incoming radio frequency (RF) signals to an intermediate frequency (IF) band. If the frequency of the local oscillator is 30 inaccurate, the translated signals may be translated outside of the desired IF band.

Digital communications systems may employ one of several methods to demodulate a digitally modulated waveform. Such methods include binary-phase-shift-keying (BPSK), quadrature-phase-shift-keying (QPSK), 35 offset QPSK (OQPSK), m-ary phase-shift-keying (MPSK), or quadrature

amplitude modulation (QAM). It is often necessary for the system to lock to a received RF signal. The ability of the modulator to lock on the signal, and therefore its performance as indicated by the degradation in the measured bit error rate (BER) versus the theoretical BER, is influenced by the phase
5 noise of the generated clock signals.

Periodic signals used in digital communications systems are often generated by a crystal oscillator having a special analog tuning circuit for adjusting the frequency of the oscillator in response to a high BER. The accompanying analog tuning circuit is typically expensive and bulky.

10 Another accurate but expensive oscillator is the voltage controlled temperature compensated crystal oscillator. These oscillators, however, used by themselves, tend to have limited frequency ranges. This often limits signal lock-on capability of a mobile receiver.

Alternatively, relatively accurate periodic signals are generated with
15 voltage controlled oscillators (VCOs) using one or more phase-locked loops (PLLs). A PLL is a circuit that outputs a signal that is phase locked to an input signal. PLLs improve frequency accuracy and lower any phase noise of a periodic signal output from a VCO and extend the range of possible output frequencies. The input signal to the PLL acts as a reference signal and is often
20 provided by another PLL, a direct digital synthesizer (DDS), a voltage controlled oscillator or a numerically controlled oscillator (NCO).

By changing specific PLL parameters such as the loop feedback divide ratio, the output frequency is adjustable in steps. The step size determines the frequency resolution of the PLL and is dependent on certain PLL
25 parameters.

Often several different frequencies must be generated from a single periodic signal to drive different local oscillators within a circuit. PLLs are often used to synthesize a range of periodic signals at precise frequencies from a single periodic signal.

30 However, a PLL driven by a conventional oscillator typically has numerous limitations. For example, the output of the PLL often contains significant spurious noise. In addition, the range of allowable output frequencies is relatively limited due to poor frequency resolution and a PLL

by itself is adjustable only in coarse frequency steps due to design limitations.

To reduce spurious noise and increase frequency resolution, two PLLs are often employed. The additional PLL provides the input or reference signal to the primary PLL and improves control over the reference frequency. This results in an output periodic signal with greater frequency resolution and accuracy.

However, the second PLL represents additional hardware that occupies valuable circuit board space and consumes power. The additional power consumption is particularly problematic in cellular telephony where the battery life of the mobile unit is an important consideration. In addition, such systems often have slow switching times causing the output of the primary PLL to wander significantly between loop corrections.

To overcome limitations associated with the use of two PLLs, a DDS is often employed in place of the second PLL, to provide the reference signal to the primary PLL. A DDS typically improves the frequency resolution and switching speed of the PLL while improving PLL design flexibility. A typical DDS driven PLL, however, has also significant limitations.

A typical DDS employs a multi-bit digital-to-analog converter (DAC). As is known in the art, multi-bit DACs have hardware limitations that result in glitches in signals output by circuits employing these devices. Glitches result when less than all of the bits in a DAC change simultaneously. Hence, the output waveform exhibits temporary false values as the bits change to their appropriate values. The glitches cause spurious frequency tones, i.e., glitch noise, to appear at the DAC output very close to the desired output frequency. The spurious tones can degrade PLL performance.

The output of the DAC also includes quantization noise that is directly related to the DAC's amplitude resolution. Amplitude resolution is determined by the number of bits used in the DAC computations. DACs with excellent amplitude resolution and frequency response tend to consume excess power and are expensive. In addition, spurious tones

become more problematic as the frequency of the periodic signal increases, further limiting the range of allowable output frequencies.

Hence, a need remains in the art for a system for providing very accurate periodic signals over a wide range of frequencies with minimal noise and fast switching speed.

SUMMARY OF THE INVENTION

The need in the art is addressed by the system for generating an accurate periodic signal of the present invention. In the illustrative embodiment, the inventive system includes a low-bit digital-to-analog converter for converting a first signal at a reference frequency to a digital signal. A delta-sigma converter is included for suppressing noise in the digital signal within a predetermined range of the reference frequency and providing a noise-shaped signal in response thereto.

In a particular embodiment, the inventive system further includes a direct digital synthesizer for providing the first signal at the first frequency. An oscillator produces an analog reference signal that is input to the direct digital synthesizer. The direct digital synthesizer converts the oscillator output signal to the first signal. The low-bit digital-to-analog converter is implemented as a delta-sigma digital-to-analog converter. In the preferred embodiment, the delta-sigma digital-to-analog converter is a one-bit delta-sigma digital-to-analog converter and includes a delta-sigma modulator with an order greater than two. The noise shaped signal is a digital signal and is filtered with a bandpass filter to remove any remaining undesirable signals such as quantization noise pushed out of band by the delta-sigma analog-to-digital converter. The output of the delta-sigma digital-to-analog converter is input to a phase-locked loop.

In the preferred embodiment, the digital-to-analog converter is a glitch-free 1-bit digital-to-analog converter. Hence, the glitch noise associated with the use of a traditional multi-bit digital-to-analog converter is eliminated. Use of a direct digital synthesizer provides for more complete control of the range of allowable frequencies for the noise shaped signal and, consequently, the frequency of the output periodic signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a signal generator comprising a direct
5 digital synthesizer (DDS) driven phase-locked loop according to the prior art.

Fig. 2 is a block diagram of a phase-locked loop synthesizer (PLL)
using a delta-sigma ($\Delta\Sigma$) modulator and a 1-bit digital-to-analog converter
(DAC) constructed in accordance with the teachings of the present
invention.

10 Fig. 3 is a block diagram of the $\Delta\Sigma$ modulator of Fig. 2.

Fig. 4 is a graph of a signal transfer function and a noise transfer
function of the $\Delta\Sigma$ modulator of Fig. 3.

Fig. 5 is a graph of the frequency spectrum of the periodic signal
output from the 1-bit DAC of Fig. 2.

15

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

While the present invention is described herein with reference to
20 illustrative embodiments for particular applications, it should be
understood that the invention is not limited thereto. Those having
ordinary skill in the art and access to the teachings provided herein will
recognize additional modifications, applications, and embodiments within
the scope thereof and additional fields in which the present invention
25 would be of significant utility.

The following review of the operation of a traditional DDS driven
PLL is intended to facilitate an understanding of the present invention.

Fig. 1 is a block diagram of signal generator 40 according to the prior
art. The signal generator 40 has a DDS 42 that is driven by a reference
30 oscillator 44. The DDS 42 synthesizes a digital signal having a frequency
dependent on the frequency of its input signal, i.e., the analog signal output
from the reference oscillator 44, and its design parameters. Construction of
the DDS 42 is well known in the art and described in U.S. Patent No.
4,965,533, entitled DIRECT DIGITAL SYNTHESIZER DRIVEN phase-locked

loop FREQUENCY SYNTHESIZER, assigned to the assignee of the present invention and incorporated herein by reference.

The synthesized digital signal is converted to an analog signal via a multi-bit DAC 46. The resulting analog signal is then filtered by a DDS filter 5 48 to remove undesirable signals such as noise and interpolate between samples to remove undesirable spectral images of the reconstructed waveform. The resulting filtered signal is provided as a reference signal input to a PLL 50.

10 The PLL 50 is a feedback loop with a transfer function designed to generate an output signal having a frequency related to the frequency of the filtered reference signal received from the DDS filter 48. The frequency of the PLL 50 output signal is a function of the parameters of the PLL 50 and the DDS 42.

15 The PLL 50 includes a phase detector implemented as a signal subtractor 78, a loop filter 80, a voltage controlled oscillator (VCO) 82, and a loop divider 84 having a divide ratio N. The PLL components 78, 80, 82, and 84 represent a feedback loop used to tune the frequency of the output periodic signal 76 to a specific synthesized frequency.

20 The loop filter 80 filters undesirable signals from the output of the subtractor 78 and then outputs a control voltage 86 to the VCO 82 that then generates the output periodic signal 76 in response to the control voltage 86. The output periodic signal 76 is fed back to the loop divider 84 that adjusts the frequency of the output periodic signal 76 in preparation for a comparison between the reference signal 74 and a divider output 88. The 25 comparison is performed by the subtractor 78 whose output is representative of the difference between the signals 74, 88 and, after filtering, results in the control voltage 86.

30 The DDS 42 provides improved frequency resolution over that of previously designed PLLs via the addition of additional design parameters provided by the DDS 42. However, as discussed above, the multi-bit DAC 46 is susceptible to glitches and spurious noise that is difficult to remove by filtering. Spurious noise and quantization noise from the DAC 46 may corrupt the output of the PLL 50.

Fig. 2 is a block diagram of a signal generator 60 constructed in accordance with the teachings of the present invention. The inventive signal generator 60 includes the reference oscillator 44 connected to the DDS 42, followed by a $\Delta\Sigma$ modulator 62, a 1-bit DAC 68, a bandpass filter 72, and 5 the PLL 50, all connected in series in the order mentioned above.

The DDS 42 driven by the oscillator 44 outputs a synthesized digital periodic signal 64 to the $\Delta\Sigma$ modulator 62. The $\Delta\Sigma$ modulator 62 acts as a noise-shaper that pushes quantization noise in the synthesized periodic signal 64 out of band, and suppresses quantization noise in band. The 10 periodic signal 64 is a digitized sine wave.

As discussed more fully below, a resonator circuit, the basic building block of the $\Delta\Sigma$ modulator 62, is characterized by the following noise transfer function:

$$15 \quad Y(z)/Q(z) = (1 + A(z)B(z))^{-1} \quad [1]$$

where z is a complex variable related to signal frequency, $Y(z)$ is the z -domain output of the basic building block, $Q(z)$ is representative of quantization noise, and $A(z)$ and $B(z)$ are functions of z designed to suppress 20 in-band quantization noise, i.e., push the noise out of band or away from the desired periodic signal frequency. In the present specific embodiment, $A(z) = z^{-1}(1+z^2)^{-1}$ and $B(z) = -z^{-1}$. Those skilled in the art will appreciate that other functions may be used for $A(z)$ and $B(z)$ without departing from the scope of the present invention.

25 The signal transfer function of the basic building block is:

$$Y(z)/X(z) = A(z)(1 + A(z)B(z))^{-1} = 1 \quad [2]$$

where $X(z)$ is the z -domain input of the basic building block.

30 As discussed more fully below with respect to Fig. 3, in the illustrative embodiment, the $\Delta\Sigma$ modulator 62 has three basic building blocks 90 cascaded together to produce a sixth order $\Delta\Sigma$ modulator 62. Those skilled

in the art will appreciate that a different order $\Delta\Sigma$ modulator may be used without departing from the scope of the present invention.

- Returning to Fig. 2, the $\Delta\Sigma$ modulator 62 outputs a noise shaped signal 66 to a 1-bit DAC 68. The $\Delta\Sigma$ modulator 62, in combination with the
- 5 1-bit DAC 68 is called a $\Delta\Sigma$ DAC. As discussed more fully below, the 1-bit DAC 68 generates considerable quantization noise. The quantization noise is suppressed in-band, i.e., near the desired periodic signal frequency. Since the 1-bit DAC 68 has only one bit, the glitch problems and resulting spurious noise resulting from the use of the multi-bit DAC 46 of Fig. 2 are avoided.
- 10 The analog output of the DAC 70 includes out-of-band quantization noise that is easily filtered out by a bandpass filter 72. Hence, the bandpass filter 72 provides a precise reference periodic signal on line 74 to the PLL 50 which lacks spurious glitch noise. The accurate reference signal allows the PLL 50 to generate accurate output periodic signals 76 over a range of frequencies by
- 15 varying the PLL 50 parameters.

As per Fig. 1, the PLL 50 includes a phase detector, i.e., signal subtractor 78, a loop filter 80, a voltage controlled oscillator (VCO) 82, and a loop divider 84 having a divide ratio N. The PLL components 78, 80, 82, and 84 represent a feedback loop used to tune the frequency of the output

20 periodic signal 76 to a specific synthesized frequency.

The loop filter 80 filters undesirable signals from the output of the subtractor 78 and then outputs a control voltage 86 to the VCO 82 that then generates the output periodic signal 76 in response to the control voltage 86. The output periodic signal 76 is fed back to the loop divider 84 that adjusts

25 the frequency of the output periodic signal 76 in preparation for a comparison between the reference signal 74 and a divider output 88. The comparison is performed by the subtractor 78 whose output is representative of the difference between the signals 74, 88 and, after filtering, results in the control voltage 86.

30 An alternative description of a phase-locked loop is provided in U.S. Patent application serial no. 08/893,267 filed July 8, 1997, entitled PHASE-

LOCK-LOOP WITH NOISE SHAPER, assigned to the assignee of the present invention and incorporated by reference herein.

The frequency of the output periodic signal F_{vco} related to the reference frequency by the following relation:

5

$$F_{vco} = F_R * N_R / (2^b) \quad [3]$$

where F_R is frequency of the reference signal 76, N_R is a frequency control variable of the DDS 42, and b is the number of bits used in the DDS 42.

- 10 Hence, the accuracy of the frequency F_R of the reference signal 74 directly affects the accuracy of the frequency F_{vco} the output signal 76.

Use of the $\Delta\Sigma$ modulator 62 and the 1-bit DAC 68 facilitates the generation of the highly accurate output periodic signal 76, lacking the spurious noise associated with expensive multi-bit DACs. In addition, the 15 spurious noise generated by the multi-bit DAC 46 of Fig. 1 does not limit the frequency of the reference signal 74. Further, the $\Delta\Sigma$ modulator 62 and the 1-bit DAC 68 are relatively inexpensive in comparison to the multi-bit DAC 46 if Fig. 1. Hence, the PLL 60 is a cost effective, highly accurate clock generation system having a relatively wide range of allowable output 20 frequencies.

Those skilled in the art will appreciate that the 1-bit DAC 68 may be replaced by a low-bit DAC such as a 2 or 3-bit DAC without departing from the scope of the present invention.

Fig. 3 is a block diagram of the $\Delta\Sigma$ modulator 62 of Fig. 2. The $\Delta\Sigma$ 25 modulator 62 is a sixth order $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator 82 has three basic building blocks 90, also termed second order resonators, cascaded together. Each basic building block 90 includes a combination of digital delays (z^{-1}) 94, amplifiers 96 having voltage gains α_i (where i is an integer index ranging from 0 to 5), an adder 98, and a subtractor 100. The adder 98 30 receives as parallel inputs, outputs from the amplifiers 96. One of the amplifiers 96 has an input provided by a digital delay 94 whose input is also the input of the other amplifier 96. This input is provided by a digital delay

94 in a subsequent resonator 90, or, in the case of the output basic block 90, provided by the noise-shaped output 66 of the $\Delta\Sigma$ modulator 82.

The first basic building block 90 receives the noise shaped signal 66 as a third input to the adder 98. Subsequent building blocks 90 receive outputs 5 of the previous basic building blocks 90 as third inputs to the adders 98.

Those skilled in the art will appreciate that methods for constructing the basic building blocks 90 are well known in the art and may be implemented via use of any digital signal processing hardware.

- The output of the adder 98 provides an input to the subtractor 100.
- 10 The output of the adder 98 is sent through a digital delay 94, providing the output of the resonator 90. The output of the resonator 90 is sent through another digital delay 94 and provides a second input to the adder 98 forming a feedback loop.

Quantization noise is modeled as a linear noise element 92 and 15 occurs before the noise shaped output 94.

The voltage gains of the amplifiers 96 are picked to provide a noise transfer function and signal transfer function that enable the $\Delta\Sigma$ modulator 82 to meet stability and noise shaping requirements for a particular application. Methods for picking of the gains α for the amplifiers 96 are well 20 known in the art. In the present specific embodiment, the gains are: $\alpha_0 = 0$, $\alpha_1 = 3/2$, $\alpha_2 = 0$, $\alpha_3 = -3/4$, $\alpha_4 = 0$, $\alpha_5 = 1/8$.

Fig. 4 is a graph 102 of a signal transfer function 104 and a noise transfer function 106 implemented by the $\Delta\Sigma$ modulator 62 of Fig. 3. The graph has an ordinate 108 representing $20\log(V)$, i.e., decibels (dB) and an 25 abscissa 110 representing frequency. The noise transfer function 106 significantly suppresses noise within a range of frequencies 112 (in-band) known as the operating region, while the signal transfer function 104 allows the signal to pass un-suppressed or even amplified. The noise transfer function 106 and the signal transfer function 104 represent noise and signal 30 gain profiles respectively.

Fig. 5 is a graph of a frequency spectrum 120 of the DAC output 70 of Fig. 2. The graph has an ordinate 122 corresponding to signal power and an

abscissa 124 corresponding to signal frequency. The spectrum 120 includes quantization noise 126 on either side of a frequency spike 128 centered at a desired output frequency 130 of the DAC output 70 of Fig. 2. The noise 126 is suppressed in-band, i.e., near the desired output frequency 130 and pushed 5 out of band. The bandpass filter 72 of Fig. 2 can then easily remove the noise 126, leaving the signal spike 128 at the desired output frequency 130. Signal energy will then be concentrated at the desired frequency 130, representing a periodic signal with excellent frequency accuracy.

Thus, the present invention has been described herein with reference 10 to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all 15 such applications, modifications and embodiments within the scope of the present invention.

WHAT IS CLAIMED IS:

CLAIMS

1. A system for generating an accurate periodic signal at a predetermined frequency comprising:
 - a low-bit digital-to-analog converter for converting a first signal at a reference frequency to a digital signal; and
 - delta-sigma means for suppressing noise in said digital signal within a predetermined range of said reference frequency and providing a noise-shaped signal in response thereto.
2. The invention of Claim 1 including a direct digital synthesizer for providing said first signal at said reference frequency.
3. The invention of Claim 2 further including a reference oscillator for providing an input to said direct digital synthesizer.
4. The invention of Claim 1 wherein said low-bit digital-to-analog converter is a delta-sigma digital-to-analog converter.
5. The invention of Claim 4 wherein said delta-sigma digital-to-analog converter operates with fewer than four bits.
6. The invention of Claim 5 wherein said delta-sigma digital-to-analog converter is a one-bit delta-sigma digital-to-analog converter.
7. The invention of Claim 4 wherein said delta-sigma digital-to-analog converter includes a delta-sigma modulator with an order greater than two.
8. The invention of Claim 1 further including synthesizing means for generating an output periodic signal from said noise-shaped signal.
9. The invention of Claim 1 wherein said synthesizing means is a phase-locked loop.

10. A system for generating a low-noise periodic signal comprising:
 - 2 digital means for generating a digital signal having a first center frequency;
 - filter means for noise shaping said digital signal to suppress noise
 - 4 around said center frequency and providing a digital output signal in response thereto;
 - 6 converter means for converting said digital output signal to an analog signal; and
 - 8 loop means for tuning said analog signal to a predetermined frequency and providing said low-noise periodic signal in response thereto.

11. The invention of Claim 10 wherein said digital means includes
 - 2 a direct digital synthesizer.

12. The invention of Claim 11 wherein said digital means further
 - 2 includes an oscillator for providing an input to said direct digital synthesizer.

13. The invention of Claim 12 wherein said oscillator is a voltage controlled oscillator.

14. The invention of Claim 10 wherein said converter means is a
 - 2 delta-sigma digital-to-analog converter.

15. The invention of Claim 10 wherein said delta-sigma digital-to-analog converter operates with fewer than four bits.

16. The invention of Claim 15 wherein said delta-sigma digital-to-analog converter is a one-bit delta-sigma digital-to-analog converter.

17. The invention of Claim 10 wherein said filter means includes a
 - 2 delta-sigma modulator.

18. The invention of Claim 17 wherein said delta-sigma modulator includes a delta-sigma modulator circuit characterized by the following signal transfer function

$$4 \quad Y(z)/Q(z) = (1 + A(z)B(z))^{-1}$$

where $Y(z)$ represents an output signal of said delta-sigma modulator circuit in the z -domain, $Q(z)$ represents quantization noise in the z -domain, and $A(z)$ and $B(z)$ are functions of z designed to suppress inband quantization noise.

19. The invention of Claim 18 wherein $B(z) = -z^2$.

20. The invention of Claim 18 wherein $A(z) = (1 + z^2)^{-1}$.

21. The invention of Claim 18 wherein said delta-sigma modulator is characterized by the following noise transfer function:

$$Y(z)/X(z) = A(z)(1 + A(z)B(z))^{-1}$$

4 where $X(z)$ represents an input signal of said delta-sigma modulator circuit in the z -domain.

22. The invention of Claim 17 wherein said delta-sigma modulator has an order greater than two.

23. The invention of Claim 22 wherein said delta-sigma modulator is a sixth order delta-sigma modulator.

24. The invention of Claim 23 wherein said delta-sigma modulator includes an amplifier with a gain of approximately 3/2.

25. The invention of Claim 23 wherein said delta-sigma modulator includes an amplifier with a gain of approximately -3/4.

26. The invention of Claim 23 wherein said delta-sigma modulator includes an amplifier with a gain of approximately 1/8.

27. The invention of Claim 10 wherein said loop means includes a phase-locked loop.

28. A system for synthesizing periodic signals at any one of a plurality of frequencies comprising;

4 an oscillator for generating a signal of a first frequency;
a direct digital synthesizer for converting said signal to a digital signal;

a delta-sigma modulator connected to receive the output of said direct
6 digital synthesizer as an input thereto;

a low-bit digital-to-analog converter for converting an output of said
8 delta-sigma modulator to an analog signal;

a filter for reducing noise in said analog signal and for providing a
10 clean reference signal in response thereto; and

a phase-locked loop having said reference signal as an input for
12 generating said one of a plurality of frequencies.

29. A system for generating a periodic signal having a specific
2 frequency comprising:

an oscillator for generating a reference signal having a frequency
4 within a specific frequency band;

noise shaping means for suppressing noise within said frequency
6 band in said oscillator signal and for providing a noise-shaped signal in
response thereto;

8 converter means for converting said noise-shaped signal to an analog
signal having low noise at a predetermined frequency; and

10 phase-locked loop means for generating said periodic signal based on
said analog signal.

30. A system for generating a periodic signal having a specific
2 frequency comprising:

a direct digital synthesizer;

4 sigma-delta digital-to-analog converter connected to receive the
output of said synthesizer as an input thereto; and

6 a phase-locked loop connected to the output of said sigma-delta
digital-to-analog converter.

31. A method for generating an accurate periodic signal at a
2 predetermined frequency including the steps of:

generating a digital periodic signal having a component at a desired
4 reference frequency;

-
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-
- suppressing noise in said periodic signal within a predetermined range of said desired reference frequency, and providing a noise-shaped signal in response thereto; and
- 8 synthesizing a periodic signal at said specific frequency based on said noise-shaped signal.

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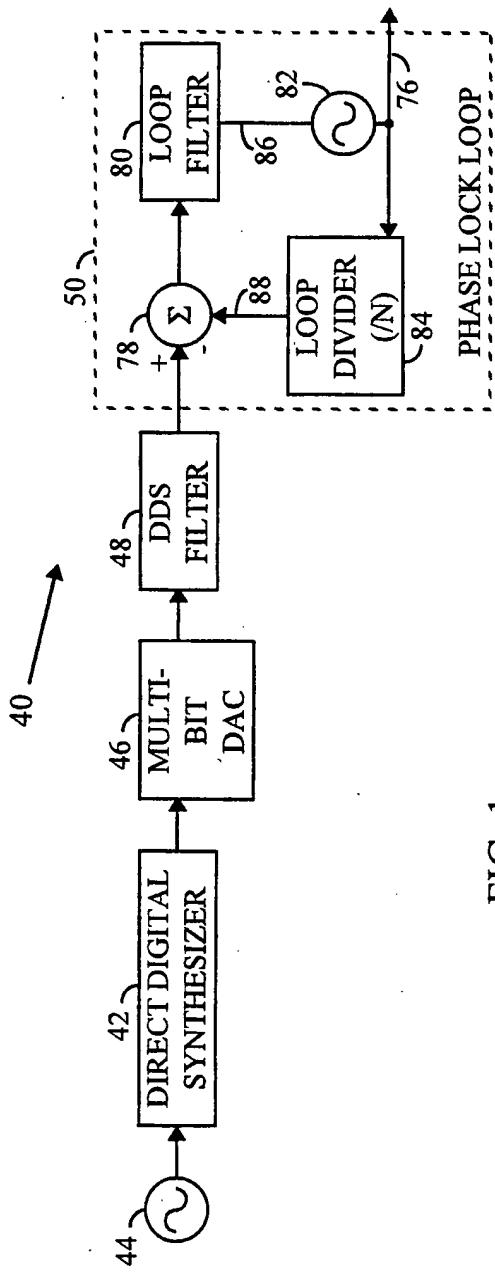


FIG. 1

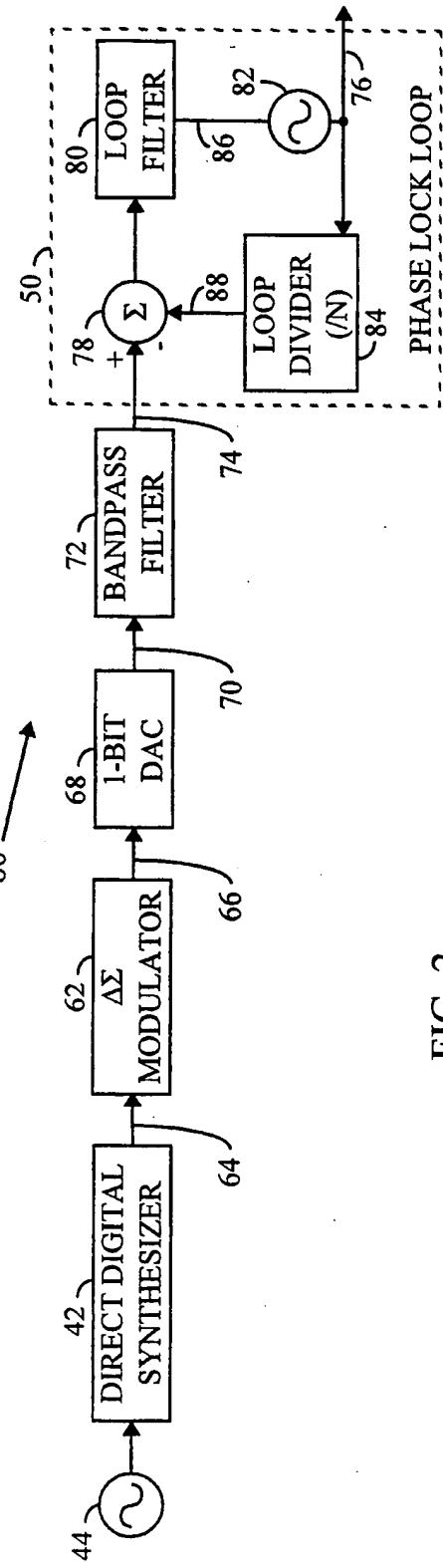


FIG. 2

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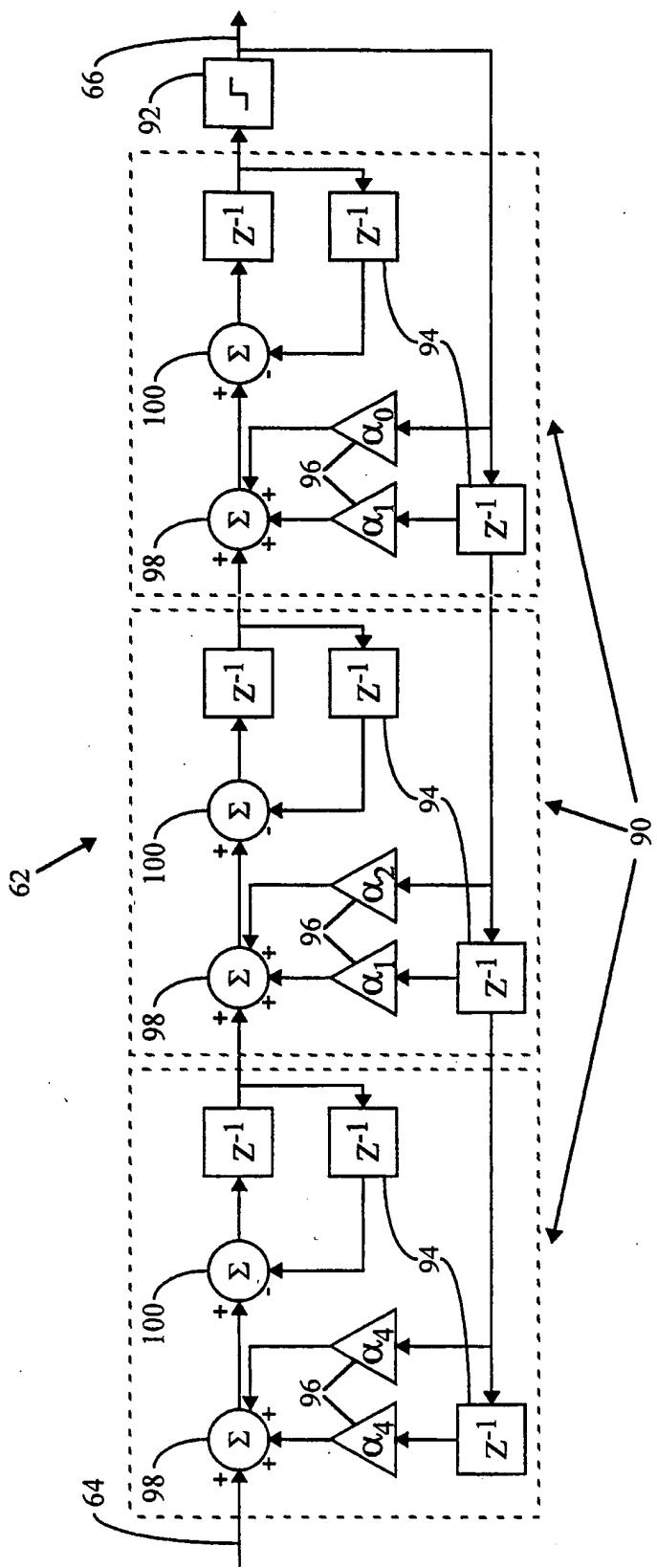


FIG. 3

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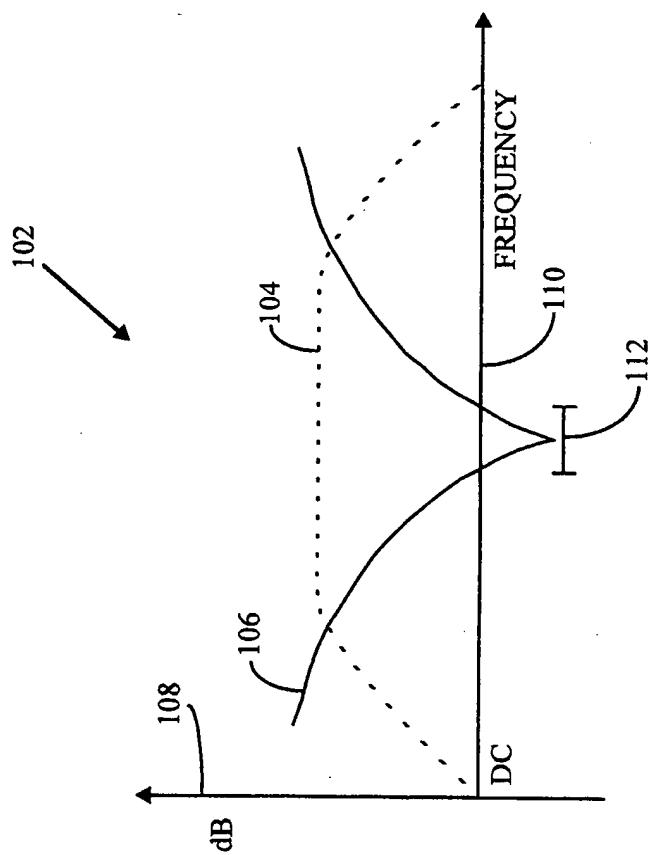


FIG. 4

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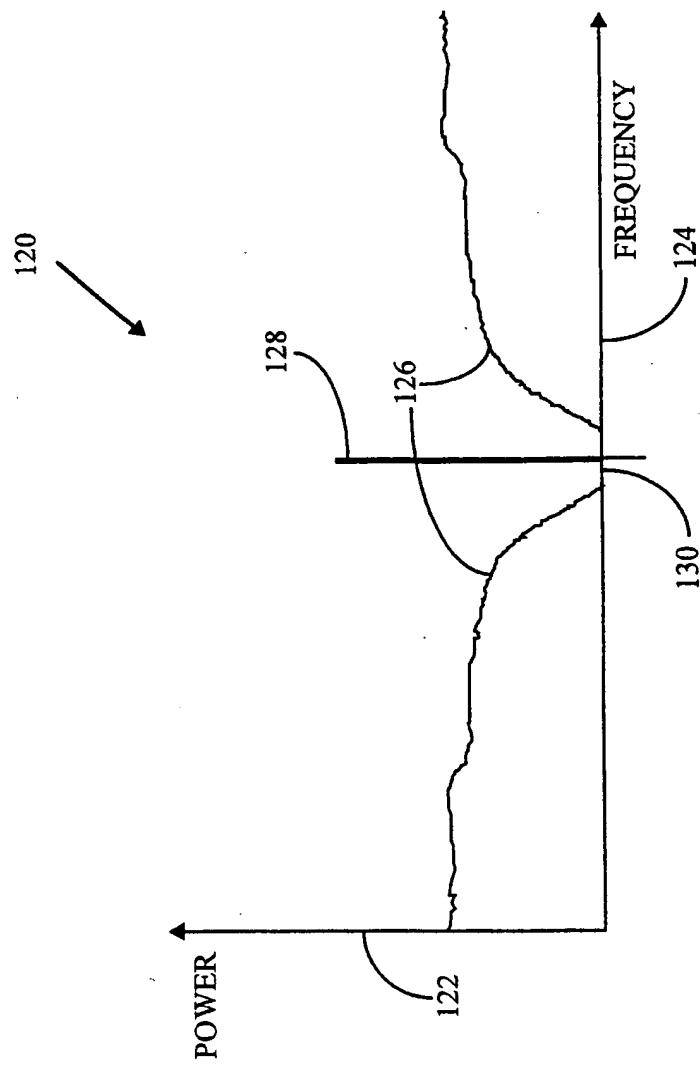


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/14655

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/18 G06F1/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>HERNANDEZ L: "FREQUENCY SYNTHESIS BASED ON BANDPASS SIGMA-DELTA MODULATION" ELECTRONICS LETTERS., vol. 32, no. 18, 29 August 1996 (1996-08-29), page 1642/1643 XP000637808 IEE STEVENAGE., GB ISSN: 0013-5194 the whole document</p> <p>---</p> <p style="text-align: center;">-/-</p>	1-31

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
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- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search	Date of mailing of the international search report
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8 October 1999

18/10/1999

Name and mailing address of the ISA	Authorized officer
-------------------------------------	--------------------

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl.
Fax: (+31-70) 340-3016

Balbinot, H

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/14655

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>DUFORT B ET AL: "SIGNAL GENERATION USING PERIODIC SINGLE AND MULTI-BIT SIGMA-DELTA MODULATED STREAMS"</p> <p>PROCEEDINGS OF THE INTERNATIONAL TEST CONFERENCE. ITC '97, WASHINGTON, DC, NOV. 1 - 6, 1997, no. CONF. 28, 1 November 1997 (1997-11-01), pages 396-405, XP000800336</p> <p>INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS ISBN: 0-7803-4210-0</p> <p>abstract</p> <p>page 398, paragraph III; figure 6B</p> <p>page 401, column 2, line 5 - line 14; figure 13</p> <p>-----</p>	1-31
A	<p>US 4 965 533 A (GILMORE ROBERT P)</p> <p>23 October 1990 (1990-10-23)</p> <p>cited in the application</p> <p>column 5, line 14 -column 8, line 54; figure 2</p> <p>-----</p>	1-3, 8-13, 27-31

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 99/14655

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4965533 A	23-10-1990 US	5028887 A	02-07-1991